Notice of Allowability	Application No.	Applicant(s)	
	10/044,295	OKAMOTO, SHIGETSUGU	
	Examiner	Art Unit	
	Nitin Patel	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/24/2004*.

2. ☒ The allowed claim(s) is/are *1-4,8-41 Now renumbered 1-38respectively*.

3. ☒ The drawings filed on *09 February 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Amare Mengistu
Primary Examiner

REASON FOR ALLOWANCE

1. Claims 1-4,8-41 are allowed. Claims 5-7 have been cancelled.

2. The prior art fails to teach or suggest a memory-integrated display element, having an optical modulation element provided in a pixel; a memory element, provided in the pixel, which stores binary data, which indicates a value inputted to the optical modulation element, wherein: the memory element is arranged by connecting at least an input inverter and output inverter to each other in a loop manner, wherein an output of the input inverter is input into the output inverter, and wherein the output inverter is a complementary inverter, and an output of the output inverter which functions as an output end of the memory element, is directly connected to one end of the optical modulation element a wherein said complementary inverter includes: a p type transistor connected to a first power line, and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter and a cathode of the optical modulation element is connected to the second power line and when a ratio of an OFF resistance-value of the n type transistor with respect to an ON resistance value of the p type transistor is K, a ratio of an ON resistance value of the p type transistor with respect to an ON resistance value of the optical modulation element is set to be substantially (K + 1)1/2/K as claimed in claim 1.

The prior art fails to teach or suggest a memory-integrated display element. comprising: an optical modulation element provided in a pixel a memory element provided in the pixel which stores binary data which indicates a value inputted to the

optical modulation element wherein: the memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner, wherein an output of the input inverter is input into the output inverter and output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element is directly connected to one end of the optical modulation element, complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line, and when a ratio of an OFF resistance value of the n type transistor with respect to an ON resistance value of the p type transistor is K, and a dispersion quantity of lighting luminance of the optical modulation element is within + x F/o with respect to a reference value, a ratio of an ON resistance value of the p type transistor with respect to an ON resistance value of the optical modulation element is set to be a range from (K + 1)1/2 * (1-x/ 100)/K to (K + 1)1/2 * (1 + x/ 100)/K as claimed in claim 8

The prior art fails to teach or suggest memory-integrated display element having an optical modulation element provided in a pixel: a memory element provided in the pixel Which stores binary data which indicates a value inputted to the optical modulation element wherein said memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner, wherein

an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element, is directly connected to one end of the optical modulation element the complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line as claimed in claim 11.

The prior art fails to teach or suggest a memory-integrated display element having data optical modulation element provided in a pixel a memory element provided in the pixel which stores binary data, which indicates a value inputted to the optical modulation element, wherein: memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner wherein an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element is directly connected to one end of the optical modulation element the complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line, and when a ratio of an OFF resistance value of the p type transistor with respect to an ON resistance value of the n type transistor is K, a ratio of an ON resistance value of

the n type transistor with respect to an ON resistance value of the optical modulation element is set to be substantially (K + 1) ½ /K as claimed in claim 12.

The prior art fails to teach or suggest a memory-integrated display element. comprising: an optical modulation element provided in a pixel a memory element provided in the pixel which stores binary data which indicates a value inputted to the optical modulation element wherein: the memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner wherein an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element is directly connected to on-e end of the optical modulation element the complementary inverter includes: a p type transistor connected to a first power line; and an n type transistor connected to a second power line, and a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line, and when a ratio of an OFF resistance value of the p type transistor with respect to an ON resistance value of the n type transistor is K, and-a dispersion quantity of lighting luminance of the optical modulation element is wihtin + x % with respect to a reference value, a ratio of an ON resistance value of the n type transistor with respect to an ON resistance value of the optical modulation element is set to be a range from (K + 1)1/2 * (1-x/ 1Oo)/K to (K + 1)1/2 * (1 + x/ 100)/K as claimed in claim 13.

The prior art fails to teach or suggest a memory integrated display element having an optical modulation element provided in a pixel a memory element provided in

the pixel, which stores binary data which indicates a value inputted to the optical modulation element, wherein: the memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner wherein an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element, is directly connected to one end of the optical modulation element the memory element includes a power electrode which is used also as either of an anode or a cathode of the optical modulation element as claimed in claim 17.

The prior art fails to teach or suggest a memory integrated display element an optical modulation element provided in a pixel a memory element provided in the pixel which stores binary data which indicates a value inputted to the optical modulation element wherein the memory element is arranged by connecting at least an input inverter and an output inverter to each other in a loop manner wherein an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element is directly connected to one end of the optical modulation element the memory element includes a first power electrode and a second power electrode, and said optical modulation element includes an anode and a cathode, and the first power electrode and the second power electrode are provided separately from the anode and the cathode as claimed in claim 19.

The prior art fails to teach or suggest a memory integrated display element an optical modulation element provided in a pixel: a memory element provided in the pixel which stores binary data which indicates a value inputted to the optical modulation element wherein the memory element is arrearage by connecting at least an input inverter and an output inverter to each other in a loop manner wherein an output of the input inverter is input into the output inverter and wherein said output inverter is a complementary inverter and an output of the output inverter which functions as an output end of the memory element is directly connected to one end of the optical modulation element further having a plurality of data signal lines; and a plurality of select signal lines which cross the data signal lines at right angle, wherein:
said memory element is provided in each of combinations of the data signal lines and the select signal lines, and stores binary data indicated by a data signal line corresponding to the memory element, in a case where a select signal line corresponding to the memory element instructs the memory element to select, and the memory element is provided adjacent to another memory element, via a reference line, either of the data signal line and the select signal line, so that both memory elements are axially symmetrical V:II respect to the reference line, and the optical modulation element is provided adjacent to another optical modulation element, via the reference line, so that both optical modulation elements are axially symmetrical with respect to the reference line, and a power line is shared by the both memory elements, or the both optical modulation elements as claimed in claim 19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 703-308-7024. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP

Amare Mengistu
Primary Examinor

October 26, 2004